Research and Development Technical Report

A FAST TURN AROUND FACILITY FOR VERY LARGE SCALE INTEGRATION (VLSI)

A SEMI-ANNUAL TECHNICAL STATUS REPORT

July 1, 1980 to December 31, 1980

DARPA Contract No. MDA 903-80-C-0432

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In order to appreciate the critical hardware and software problems associated with the definition and design of very large scale integrated circuits or integrated systems including 10^4 - 10^6 transistors in a single silicon chip, incisive experiments conducted with actual operating chips are indispensible. The objective of this project is to establish within a university research environment, a facility for the rapid execution of mask generation, wafer fabrication, and functional testing of user-generated custom I. C. designs.

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Research Project

A FAST TURN-AROUND FACILITY FOR VERY LARGE SCALE INTEGRATION (VLSI)

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INTRODUCTION

This document is the first semi-annual report for the Stanford University Fast Turn Around Facility project DARPA Contract No.: MDA 903-80-C-0432 covering the period July 1, 1980 to December 31, 1980.

SUMMARY

7/1/80 to 12/31/80

SUMMARY

This document describes activity in the DARPA sponsored Fast Turn-Around Facility for VLSI Project during the period July 1, 1980 to December 31, 1980. The principal goal of the FTAF is to provide fast turn-around fabrication of silicon integrated circuits for the local VLSI design community. The Stanford Integrated Circuits Laboratory (with close cooperation from Stanford's Information Systems Laboratory and Computer Systems Laboratory) has been actively pursuing many of the practical aspects of producing small numbers of custom designed integrated circuits with a short turn around time. This report will focus on many of the facilities, equipment, and fabrication issues which affect our ability to fabricate and test these custom designed chips.

The FTAF Project is organized into the following four major activities:

FTAF Wafer Fabrication

Electron Beam Lithography

Electrical Wafer Testing

VLSI Device Research

More detailed descriptions of each of these four areas appear as individual sections later in this report. However this summary will describe the important activities and results in each of the four areas that have occurred during the past six months.

The FTAF wafer fabrication activity has focused on establishing a "baseline" NMOS enhancement/depletion process schedule which will be suitable for circuits designed using the Mead-Conway design methodology. This is a fully ion implanted process having the following main features:

(1) Locally oxidized channel stop/field oxidation resulting in field thresholds and diode breakdowns of 18 volts. These voltages are sufficiently high to allow circuit operation at the standard TTL voltage level of 5 volts with ample safety margin.

(2) Shallow arsenic source and drain regions to minimize the gate/drain overlap capacitance and therefore improve the high speed performance of the process.

(3) Thin gate oxide and a boron drain/source punch-through prevention implant for compatability with channel lengths of 2-3 microns although our initial patterning limits will cause us to use minimum feature sizes of 5 microns.

It should be emphasized that these three features are important because the resulting process schedule should be compatible with future reductions in feature size without redesigning the process. Specifically, the Stanford University NMOS enhancement/depletion process should be compatible with minimum feature sizes of 2-3 microns -- the percent process should be suitable for FTAF wafer fabrication until the end of Stage 2 of the present DARPA contract (i.e. September 30, 1982). A complete process description appears in the detailed FTAF Wafer Fabrication section of this report. The process requires six masks (including scratch mask protection) and results in enhancement transistor thresholds of +0.8 volts and depletion transistor thresholds of -3.0 volts.

As previously mentioned, the circuits which we have fabricated to date have had minimum feature sizes of 5 microns. The use of wet etching (as opposed to "dry" plasma etching techniques) has prevented the use of feature sizes less than 5 microns. We have recently installed, and are in the process of evaluating, a Plasma Therm PK 12 parallel plate plasma reactor. Initially we are investigating the use of plasma etching of the polysilicon layer, because it is the layer which has the greatest impact on the operating speed of NMOS devices and therefore must be the most precisely controlled. In addition to

etching technology, we must of course be able to precisely produce the desired patterns in photoresist. At present, we are using a Canon FPA 141 reducing projection printer and AZ 1470 J positive photoresist in our lithography area. Taken together, we are able to resolve patterns in photoresist with feature sizes of less than two microns, which again is suitable through Stage 2 of the present DARPA contract.

One of the most important aspects of wafer fabrication is the reduction of the defect densities to a sufficiently low level that we may successfully fabricate larger and larger circuits. Particularly in the university environment, the control of defect densities poses a significant set of problems. Recent improvements to the overall cleanliness of our wafer fabrication facility include the addition of an automatic emulsion plate processor for producing emulsion photomasks with fewer defects, and extensive additions of HEPA laminar flow air modules to decrease the density of airborne particles.

We have spent a great deal of effort on the evaluation and selection of an electron beam lithography system. We have selected the ETEC MEBES system for reasons which are detailed in the electron beam lithography section of this report. Initially, the MEBES system will be used as a high quality mask generation system; however, we ultimately plan to use this system for directly exposing resist on wafers. It should be pointed out that none of the commercially available electron beam lithography systems currently guarantee a direct write capability -- ETEC, however, has undertaken a joint development program with us which will result in direct-write capability with a minimum feature size of 1/8 micron. The MEBES system has been constructed and has successfully written patterns in resist at the ETEC factory in Hayward, California.

Activity in the area of wafer testing has concentrated on two aspects of testing: (1) the selection and purchase of a general purpose digital tester for functional testing of complete circuits and (2) design and fabrication of test structures which will characterize important DC and AC aspects of the current NMOS process. As indicated in the detailed report on testing, we selected the Tektronix S3260 test system primarily because it was the most versatile and flexible system available at the time. In the area of device and process characterization, we have developed two sets of masks which allow us to study and monitor the properties of the current NMOS enhancement/depletion process. In addition to a complete family of DC test vehicles (including enhancement and depletion test transistors, polysilicon and diffusion resistances, crossover and contact hole integrity checks, etc.), we have included a variety of AC performance test vehicles. For example, we have included a family of ring oscillators with varying degrees of parasitic interstage loading (both resistive and capacitive) to better understand the high speed capabilities of our process. It is well known that a simple ring oscillator generally provides an overly optimistic estimate of circuit performance because it doesn't accurately simulate the parasitic loading encountered in REAL circuits.

In conclusion, activity during the initial period under DARPA support has concentrated on establishing the technology and support structures which will be required to meet the overall goals of this program -- namely, quick-response fabrication of integrated circuits based on designs generated by the local VLSI design community. Among the accomplishments or highlights of this initial reporting period are:

(1) Establishment of a baseline NMOS enhancement/depletion process which will be suitable for minimum feature sizes in the 2 - 3 micron range. (Although present etching technology limits us to 5 microns)

(2) Selection and purchase of an ETEC MEBES system to be used initially for writing high resolution mask patterns and ultimately for the direct writing of patterns on resist-coated wafers.

(3) Initiation of a series of activities which will enable us to reduce the minimum feature size and the density of fabrication defects to allow us to fabricate more complex circuits.

(4) Selection and purchase of a general purpose test system for the functional evaluation of completed designs.

(5) Design and fabrication of process and device test structures to allow us to monitor our process control and to provide the circuit/system designers with the appropriate set of device characteristics.

The first three of these achievements are significant, we feel, because they attack the fabrication and technology aspects of providing a state-of-the-art process capability for the system design community. The final two highlights of this initial reporting period are equally significant in that they represent our strong commitment to the development of a suitable testing and characterization "environment" which will streamline the design-simulation-fabrication-testing sequence.

Finally we would like to acknowledge that the FTAF fabrication project depends heavily on strong interactions with a variety of other research groups: in particular, much of our technology development is coupled to and complemented by a strong program in process modeling which has been supported by Dr. Dick Reynolds of DARPA for several years. We have also enjoyed close interactions with Stanford's Information Systems and Computer Systems Laboratories -- in particular with John Newkirk and Rob Mathews in the area of wafer testing.

FTAF WAFER FABRICATION

7/1/80 to 12/31/80

Fast Turn-Around Facility (FTAF)
At Stanford University
Interim Progress Report - November 13, 1980

Submitted by J. D. Shott and J. D. Meindl

The Integrated Circuits Laboratory at Stanford University has recently (~ October 1, 1980) received funding support from DARPA to provide fast turn-around fabrication of silicon integrated circuits for the local VLSI design community. Initial activity on this project has concentrated on establishing a baseline NMOS process technology (λ = 2.5 μm) and on establishing the necessary support structures (software, hardware, facilities, etc.) to allow us to convert a CIF design file into a set of photomasks, fabricate wafers using those photomasks, and provide packaged, testable chips for the designer with our most closely coupled members of the design community: Rob Mathews and John Newkirk of ISL and Jim Clark of CSL at Stanford.

The description of recent activity relating to the Fast Turn-Around Facility will be partitioned into the following four categories:

Facility Improvements

NMOS Process Refinements

Process Characterization and Testing

Interactions with ISL and CSL at Stanford.

Facility Improvements

Successful achievement of the goals of the FTAF will require lower defect densities and greater process line reliability than ever observed in a university integrated circuit facility. Reducing defect densities and

increasing process line reliability are both tasks which call for sustained engineering effort. We are presently augmenting our manpower pool of research staff, technicians and graduate students with additional engineering/maintenance support.

The Integrated Circiuts Laboratory is presently located in a building that does not provide adequate environmental control for the fabrication of large integrated circuits. Although fund raising for an improved facility is proceeding rapidly, we have recently completed (and continue to pursue) modifications to the physical plant which will enhance our ability to produce low defect density integrated circuits. In particular, we extensively modified the air handling system in the building to provide "clean" air in the critical processing areas devoted to mask making, photolithography, and wafer cleaning. Airborne particulate matter is the primary source of defects in any of these areas. Although these areas are still not as clean as one would expect for a properly designed, industrial integrated circuit facility, we were successful in reducing the concentration of airborne particulates in these areas by roughly three orders of magnitude.

At present, facilities are being prepared which will provide a "hyper-clean" environment for the electron-beam lithography system and associated resist processing equipment which will be delivered in mid-1981. To make room for this equipment, support equipment such as DI H_2O, LN_2, LO_2, LAr, and compressed air systems are all being relocated outside the building.

NMOS Process Refinements

We are presently fabricating NMOS integrated circuits using an enhancement/depletion polysilicon gate technology with minimum feature sizes of 5 μm (λ = 2.5 μm) and with a single level of Aluminum metallization. We currently

have a number of projects under way which will either improve the performance (for the same geometries) of the current NMOS process, reduce the defect densities in the process (and allow us to make bigger chips), decrease the turn-around time through the lab, decrease the minimum feature sizes allowed, or develop new technology which may be useful to the design community. A brief summary of many of these activities follows:

In the area of maskmaking and photolithography we are currently loading CIF tapes into an Applicon Graphics Design System which produces a sorted, David Mann-compatible pattern generator tape. This is turn drives a David Mann 1600 pattern generator which produces a 4:1 emulsion reticle for use on our Canon 4:1 reducing projection alignment system. Recent improvements in the Applicon sorting algorithm have doubled the flash rate of the pattern generator to roughly 2000 flashes per hour. Installation of an emulsion plate processor has resulted in reduced defect densities on the emulsion reticle and, by allowing "reversal" processing of the photoplates, makes it possible to use positive photoresist throughout the fabrication sequence. The use of positive resist becomes virtually mandatory as minimum feature sizes shrink much below 5 μm.

For the production of large circuits with small feature sizes in a short time, electron beam lithography is far superior to optical pattern generation techniques. An electron beam lithography system has been purchased from ETEC and should be delivered by mid-1981. Initially this system will be used for the generation of high quality 4:1 chrome reticles for use on the Canon projection alignment system. Ultimately, as the technology matures, we plan to use the ETEC system to directly expose resist coated wafers. At the present, we are preparing our facility to accept the electron beam system and are involved in a training program at ETEC to learn how to operate and maintain this delicate system.

Our minimum feature size of 5 microns is not limited by our ability to resolve patterns in photoresist, but rather is limited by the isotropic etching characteristics provided by wet chemical etchants. Within the last month we have installed a Plasma Therm parallel plate "dry" etching reactor. Initial experiments are under way to characterize the system, particularly for etching the polysilicon and phosphosilicate glass layers in the NMOS process. Under the proper conditions, dry etching is known to produce precisely controlled, anisotropic etching characteristics. Because of cross-contamination of various etchant gases, plasma etching of aluminum must await the purchase and delivery of a second plasma etching system.

In order to reduce defect densities associated with the high temperature steps of diffusion, oxidation, and chemical vapor deposition, we have purchased and are in the process of installing a new bank of furnaces to be used for diffusion, oxidation, and polysilicon low pressure chemical vapor deposition (LPCVD). To reduce defect densities associated with particulate matter, all wafers will be held vertically in these furnace systems. Furthermore, to enhance the chemical cleanliness of these systems, all furnace tubes are equipped with HCl "gettering" systems and the oxidation furnaces have clean "pyrogenic" steam systems.

New technologies other than single-level metal NMOS are also being supported by DARPA. Areas under investigation include buried channel MOS transistors, static induction transistors, high performance CMOS, and multi-level metal interconnections. These technologies are in the early phases of development at Stanford, but are ultimately targeted for release to the design community.

It should be pointed out that much of our technology development is coupled to and complemented by a strong program in process modeling which has been supported by Dr. Dick Reynolds of DARPA for several years. Of

particular interest to us is the work aimed at better understanding the growth of thin films of SiO_2, the growth and doping of poly-silicon, the properties of WSi_2 as a low resistivity gate electrode, and the incorporation of this understanding into the process simulator SUPREM.

Process Characterization and Testing

Since the start of the FTAF project, two sets of test chips have been designed, with the first set already fabricated and tested. The first set provided basic process development information and demonstrated functional capabilities. Since the spring of 1980, a second test chip set has been designed and is currently in fabrication after its completion in September. This chip set refines the test device complement to include more sophisticated measurements, and incorporates several examples of end user oriented circuits.

The second test chip set is a 9 by 9 mm matrix, containing six 3 by 3 mm chips with test devices, and one 3 by 9 mm chip with a self-scanned 700-element linear sensor array. Simple test devices provided include capacitors, resistors, transistors, inverters, and crossover and contact strings. There are also devices provided for the electrical measurement of alignment, poly-silicon signal delay, and channel width and channel length effects on device properties. Complex active test circuits include digitally controlled wide-band amplifier cascades, amplifier scaling tests, high performance operational amplifiers, and static and dynamic BCD counters.

The 700-element self-scanned linear sensor array is custom designed specifically to meet the requirements of a DARPA supported surface acoustic wave convolver device under development in Dr. Kino's laboratory. This device has interleaved sensing diodes on a 10μ pitch, and a dynamic shift register to control multiplexing of the diode charges onto a common analog bus. Space is

provided for integrated acoustic transducers on the chip at each end of the sensor line array.

Future plans are to continue evolution of the test chip set content to maximize information about the process performance, as well as including devices to service specific user group needs. An area of new work is the development of cellular active yield test chips specifically oriented towards measurement with a computerized VLSI test machine.

A second endeavor is the selection, installation, and use of a computerized VLSI test machine to enable rapid and accurate characterization and selection of chips produced for users. To this end, a detailed study of commercially available machines was concucted jointly with members of ISL ending in selection of the Tektronix S3260 as most suited to our needs. This machine has been procured for installation in December, 1980, and will be integrated into the other computerized design and test facilities already present at Stanford.

Interactions with ISL and CSL at Stanford

Because of the interdisciplinary nature of many of the obstacles to rapidly designing, fabricating, and testing integrated circuits, we in the Integrated Circuits Lab, the Information Systems Lab, and the Computer Systems Lab at Stanford are attempting to coordinate our efforts as much as possible. As previously mentioned, we have jointly been involved in the selection of a Tektronix digital testing system and in the conversion of CIF design files into Applicon-compatible format tapes in order to "fracture" the patterns for use in the pattern generation process.

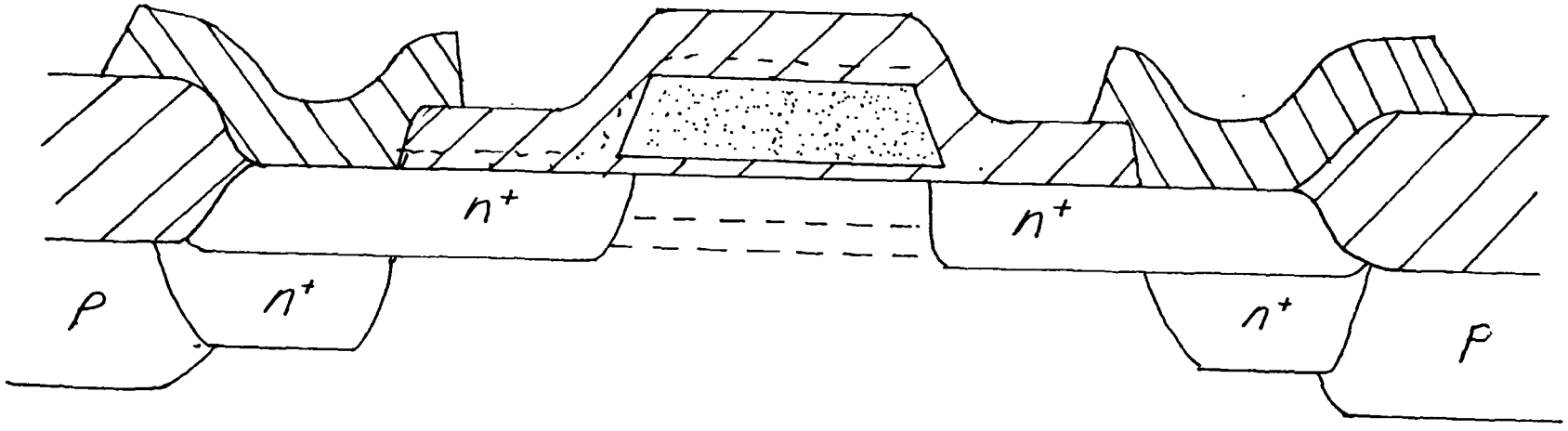
We are currently planning to fabricate wafers for Jim Clark and for the fall quarter Newkirk/Mathews VLSI design course. In either case, the

complexity of these devices is sufficient to make it impractical to use our David Mann optical pattern generator to fabricate these masks. We are discussing with ETEC the possibility of generating these masks on one of their machines as a portion of our training program. If this works out, device fabrication will be scheduled for mid-December.

As the size of the chips increases, it becomes less desirable to use magnetic tapes and the Applicon as intermediate steps between the design file and the E-Beam lithography system. As a result, we are jointly exploring the hardware and software requirements involved in coupling the ISL VAX to the Eclipse in the ETEC electron beam lithography system.

In conclusion, the Integrated Circuits Lab (with close cooperation from Stanford's ISL and CSL) has been pursuing and will continue to pursue many of the practical aspects of producing small volumes of custom designed integrated circuits with a short turn-around time. The next major fabrication milestone will be the fabrication of the chips designed by Jim Clark and by the Newkirk/Mathews VLSI design class in mid-December 1980.

SU ENH/DEPL NMOS



$X_o \approx 750$ Å

$X_J \approx 0.4$ µm (As)

FULLY ION IMPLANTED

HIGH D/S PUNCHTHROUGH

John Shott
Charlie Ho

NMOS V

1. Backside implant damage gettering
   Ar^{40} - 3 x 10^{15} cm^{-2} @ 180 KeV

2. Ar/HCl pre-oxidation gettering
   30 min @ 850°C - Ar + 0.5% O_2 + 0.5% HCl
   Ramp up to 1250°C in Ar/O_2/HCl ambient
   Switch to O_2 + 0.5% HCl for 1 hr
   Ramp down to 850°C in O_2/HCl ambient

3. Post-oxidation
   1000°C dry O_2 + 1% HCl - 70 min
   x_o ~750 Å
   (no HCl: 1000°C dry O_2 - 100 min; x_o ~740 Å)

4. Si_3N_4/SiO_2 deposition
   800 Å Si_3N_4 @ 955°C + 400 Å SiO_2 @ 860°C
   (uncorrected pyro on wafer)

5. Si_3N_4/SiO_2 densification
   950°C - 60 min dry O_2

6. Field lithography

7. Masking oxide etch
   1 min 6:1 BHF

8. Photoresist rebake
   30 min @ 120°C

9. Channel stop implant (through nitride/oxide)
   B" - 1.5 x 10^{13} cm^{-2} @ 160 KeV

10. Resist strip and clean
    Resist strip ($H_2SO_4/H_2SO_4 + H_2O_2$)
    50:1 HF dip ~10 sec

11. Etch nitride/etch oxide
    Refluxed H_3PO_4 ~155°C - 25 min
    6:1 BHF ~1.5 min

12. Anneal implant and field oxidation

    1000°C - 15 N_2 - 10 DO_2 - 180 WO_2 - 10 DO_2

    x_o ~7200 Å

13. Strip oxide/strip nitride

    50:1 HF dip ~3 min

    Refluxed H_3PO_4 ~155°C - 25 min

14. Enhancement implants

    Deep B" - 1.5 x 10^{11} cm^{-2} @ 120 KeV

    Shallow B" - 3.0 x 10^{11} cm^{-2} @ 35 KeV

15. Depletion lithography

16. Depletion implant

    P^{31} - 1.2 x 10^{12} cm^{-2} @ 100 KeV

17. Resist strip and clean

    Full prediffusion clean (no 50:1 dip; isopropyl dry)

18. Poly deposition

    5 min deposition @ 900°C

    x_{poly} ~4500 Å

19. Poly doping

    30 min $POCl_3$ @ 975°C

    Bubbler N_2 set @ 5/room temperature water bath

20. Poly masking oxidation

    800°C 5 min DO_2 - 20 min WO_2 - 5 min DO_2

    x_o ~750 Å

21. Poly lithography

22. Masking oxide etch

    6:1 BHF ~1.5 min

23. Resist strip and clean

    Full prediffusion clean (50:1 HF dip ~10 sec)

24. Poly etch

    200:1 HNO_3:NH_4F with burst N_2 ~3 min

25. Unmasked oxide etch/pre-implant clean
    5:1:1 DI H_2O/HCL/H_2O_2
    10:1 HF ~3 min

26. Drain/source implant
    As^{75} - 6 x 10^{15} cm^{-2} @ 100 KeV

27. Implant anneal/oxidation
    30 min N_2 - 60 min WO_2 - 10 min DO_2 @ 800°C
    x_o (D-S) ~1200 Å
    x_o (poly) ~1500 Å

28. Contact #1 lithography

29. Contact #1 etch
    6:1 BHF ~2.5 min

30. Backside etch
    Protect frontside
    6:1 BHF ~5 min backside

31. Phosphorus-glass deposition
    Prediffusion clean (no 50:1 HF dip; isopropyl dry)
    Load wafers on 3" dummy substrates
    Deposition: 24 min @ 450°C
    x_{glass} ~6000 Å
    Conditions: Silane = 40 glass @ 5 psi
    PH_3 (1%) = 15 ss @ 15 psi
    O_2 = 12 glass @ 15 psi
    N_2 = N_2 (diluent) = 10.5 ss @ 20 psi

32. P-glass densification
    30 min N_2 @ 900°C

33. Contact #2 lithography

34. P-glass etch
    Vapox etch ~2.5 min

35. Backside implant damage gettering
    Ar^{40} - 3 x 10^{15} cm^{-2} @ 180 KeV

36. P-glass reflow
    Prediffusion clean (no 50:1 HF dip; isopropyl dry)
    30 min @ 1000°C in phosphorus predep tube in N_2 (no $O_2/POCl_3$)

37. Contact flash etch
    50:1 HF dip ~30 sec
    Isopropyl dry

38. Poly deposition
    1 min @ 900°C
    X_{poly} ~800 Å

39. Poly doping
    30 min $POCl_3$ @ 900°C
    Bubbler N_2 = 5/room temperature water bath

40. P_2O_5 strip
    50:1 HF dip ~1.5 min

41. Al metallization
    1.0 μ - E-beam (planetary @ maximum speed)

42. Metal lithography

43. Al etch
    ~2.5 min @ 43°C

44. Resist strip
    Ecostrip + solvent clean

45. Poly etch
    100:1 HNO_3:NH_4F ~1 min

46. Forming gas anneal
    Solvent clean + 50:1 HF dip ~10 sec
    1 hr @ 450°C in forming gas

47. Silox deposition
    Load wafers on 3" dummy substrates
    Deposition: 20 min @ 450°C
    X_{silox} ~1 μ
    Conditions: Silane = 75 glass @ 5 psi
    PH_3 (1%) = 4 glass @ 15 psi for first 15 min

47. Conditions: O_2 = 12 glass @ 15 psi
N_2 = N_2 (diluent) = 10.5 ss @ 20 psi

48. Scratch mask lithography

49. Silox etch
Vapox etch ~4 min

50. Resist strip
Ecostrip + solvent clean

ELECTRON BEAM LITHOGRAPHY

7/1/80 to 12/31/80

MEBES

7/1/80 - 12/31/80

ELECTRON BEAM PATTERN GENERATION

An outline specification was circulated to five manufacturers of electron beam pattern genertaors (EBPG). The specification called for an instrument capable of routinely and reliably writing high quality, highly complex photolithographic masks and which could also directly write on resist coated wafers for the fabrication of VLSI circuits with submicrometer dimensions.

The response indicated that such a machine was not available. In August we wrote up descriptions of acceptance tests for available machines. The selection committee settled for the Perkin Elmer MEBES which enjoyed a good reputation as a mask maker, which could be used for direct writing and had the promise of being extended to better resolution than that specified on the current model.

The system was assembled and integrated by the end of November 1980; at that time a beam diameter of 0.125 micrometer was demonstrated on the standard column. A set of acceptance tests, including the direct writing of two levels of a Stanford multi project chip, was drawn up for the ETEC MEBES machine. We have also designed a preliminary layout for the MEBES in the basement of McCullough in the IC Lab.

In May a letter was addressed to five suppliers of electron beam pattern generators outlining our requirements for a system which would generate reticles, 1:1 master masks, and which could also be used eventually for the direct fabrication of VLSI circuits with 1/2 μm features by direct exposure of resist control wafer. This last requirement implied a beam resolution and address size of 0.125 μm or smaller.

Proposals wre received during June and early July from three companies:

Perkin Elmer - ETEC
Philips Instruments
Varian Associates (Extrion Division) (2 proposals)

A meeting was held on July 14 to discuss the three proposals. Present were J. D. Meindl, John Shott, Jacques Beaudouin, R. F. W. Pease, David Dameron. The Varian proposals were first discussed; one of them, or a prototype instrument was considered unacceptable because: 1) the system described was a 1 on only 2 made and therefore would lack a large user community with the attendant difficulties of maintenance and upgrading, 2) there was no mention of a 0.125 μm capability on the instrument.

The second proposal from Varian was for a current production system. The specification of the system indicated that it should be able to perform the mask making tasks but again the proposal made no mention of a 0.125 μm capabilty. It was believed that a similar system (with 40 MHz capability) was being installed at Fairchild but had not yet passed acceptance tests.

The Philips proposal was next discussed together with the results of previous meeting between members of Philips (Jim Alexander) and of SEL (Meindl, Beaudouin, Pease, Shott). On paper this instrument should meet out requirements but the actual performance of the instrument in the U.S. (at Signetics) and so far been disappointing. Although 10x reticles are satisfactory, 1:1 masks have not been acceptable and no direct write capability is yet available on the instrument at Signetics.

The Perkin Elmer - ETEC proposal described a system which definitely should meet out mask making requirements because of the many (in excess of a

dozen) systems already installed and performing satisfactorily. A limited direct write capability already exists on these instruments but as delivered they do not have a 0.125 μm capability. Perkin Elmer indicated that they had a suitable development program and such a capability should be retrofitable. Perkin Elmer also expressed a strong interest in cooperating with Stanford in developing electron lithography for submicron VLSI fabrication using the delivered system.

In the following discussion several points emerged:

(1) The price tag on the 2nd Varian System and on the Philips and Perkin Elmer systems were all very similar -- $1.8M for a basic machine rising to $2M with various options.

(2) It would be attractive to deal with a supplier who was geographically nearby.

(3) Up-time was an important parameter which was mentioned in none of the proposals.

(4) Delivery time for the 2nd Varian system was 12 months After Receipt of Order; for the Philips instrument, 7-8 months; and for the Perkin Elmer instrument, 6 months.

The advantages and disadvantages of each system were discussed. It was decided that the Perking Elmer - ETEC proposal was the most attractive. The reasons for the choice of the Perkin Elmer proposal are:

(1) The strong record of performance of a large number of similar instruments in the field. This not only assures that the instrument performs but also provides a large user community.

(2) The nearby geographical location (Hayward, California) of the vendor's plant.

(3) The proven potential for high resolution (0.125 μm of an instrument of the type proposed.

(4) The rapid delivery time (6 months After Receipt of Order).

(5) The strong interest expressed by top management in cooperating with Stanford on using a delivered instrument for developing electron lithography for submicron VLSI fabrication.

FTAF WAFER TESTING

7/1/80 to 12/31/80

FTAF TESTING ACCOMPLISHMENTS

7/1/80 - 12/31/80

Since the start of the FTAF project, two sets of test chips have been designed. The first set provided basic process development information and demonstrated functional capabilities. A second test chip set has been designed which refines the test device complement to include more sophisticated measurements, and incorporates several examples of end user oriented circuits.

The second test chip set is a 9 by 9 mm matrix, containing six 3 by 3 mm chips with test devices, and one 3 by 9 mm chip with a self-scanned 700-element linear sensor array. Simple test devices provided include capacitors, resistors, transistors, inverters, and crossover and contact strings. There are also devices provided for measurement of electrical alignment, polysilcon signal delay, and channel width and channel length effects on device properties. Complex active test circuits include digitally controlled wideband amplifier cascades, amplifier scaling tests, high performance operational amplifiers, and static and dynamic BCD counters.

The 700-element self-scanned linear sensor array is custom designed specifically to meet the requirements of a surface acoustic wave convolver device under development in Dr. Kino's laboratory. This device has interleaved sensing diodes on a 10μ pitch, with a dynamic shift register controlling multiplexing the diode charges onto a common analog bus. Space is provided for integrated acoustic transducers on the chip at each end of the sensor line array. This chip was also fabricated by itself on several wafers to give a maximum number of die for testing.

Preliminary tests of fabricated test chips have concentrated on the operational amplifiers and linear sensor. The operational amplifiers yielded

performance similar to the predictions from their SPICE simulation, with excellent gain and output voltage range. The linear sensor operated as designed, with a yield of 20% fully functional devices. These devices are now being used as starting material for fabrication of the acoustic convolver. Future plans are to continue evolution of the test chip set content to maximize information about the process performance, as well as including devices to service specific user group needs. An area of new work is the development of cellular active yield test chips specifically oriented towards measurement with a computerized VLSI test machine.

The current test mask design contains seven separate chip designs. These are:

1) MOSTEST 1; with test capacitors for all layers; polysilicon, diffusion and metal resistors; enhancement and depletion transistor pairs; and enhancement transistors size test.

2) MOSTEST 2; with 4 types of crossover and contact string tests; electrical alignment tests for all mask alignment steps; and 7 each enhancement and depletion transistors with a 5μ channel width and a 1.25μ to 5μ channel length.

3) MOSTEST 3; with two ring oscillators for measuring polysilicon line delay times; 7 each enhancement and depletion transistors with 1.25μ to 5μ channel width and 5μ channel length; and 5 variations on a precision NMOS operational amplifier.

4) AMPTEST 1; with digitally controlled wideband amplifier cascades; 1 stage 20μ line width; 6 stage 10μ line width; 6 stage 5μ line width; and a preamplifier bias generator.

5) AMPTEST 2; with a 12 stage preamplifier cascade using 5μ rules; a long dynamic shift register on 5μ rules; and one decade of a BCD counter using a static D type FF binary design.

6) COUNTER; a complete microprocessor interfaced seven digit BCD frequency and event counter chip, containing both static and dynamic BCD counter stages.

7) SENSOR; an NMOS implementation of a line image sensor similar to one made by Reticon; the principal changes being to use 5μ by 1 mm detector diodes on a 10μ pitch instead of wider diodes on a 40μ pitch and implementation in NMOS instead of the original PMOS technology. A total of 700 sensor diodes are provided in a 7 mm long array with self-scanning shift register logic.

CHOICE OF IC FUNCTIONAL TEST AND MEASUREMENT SYSTEM FOR STANFORD ELECTRONICS LABORATORIES

Irene M. Watson

Jointly, Terry Walker, Robert Mathews, John Newkirk, and I prepared a set of specifications for an IC tester for the fast-turn-around fabrication system. See Appendix 1 for a list of these specifications. The primary requirement is for a general-purpose tester able to functionally test and measure any type of MSI, LSI, or VLSI circuit with up to 64 pinouts.

In June and July, 25 companies who sell IC test equipment were contacted. Literature was solicited from each vendor. From these contacts we found that only 19 of these companies sell IC testing systems and only 8 of these sell general-purpose, functional-test and measurement systems. See Appendix 2 for a list of the companies by tester type.

Of the 8 companies that sell general-purpose systems, 2 sell testers only suitable for testing MSI circuits, 2 sell small, production-oriented, bench-top LSI testers not suitable for our situation, and 4 sell LSI-VLSI testing systems. See Appendix 3 for a categorization of these 8 systems.

Of the 4 LSI-VLSI testing systems, only the Tektronix and the Fairchild systems appear to give us the flexibility we need in a research and development environment; the Megatest and Teradyne systems are both oriented to a production environment. Both the Fairchild and Tektronix systems are stand-alone computer syustems that connect to a table containing the pin electronics. The pin electronic PC boards are in a carousel organization with the socket for the device under test in the center. Both systems include a control CRT terminal, a line printer, an RS232 communications interface, disk storage, timing generators, power supplies, a wafer prober interface, an

operating system, utility programs, and a high-level testing applications language. The Fairchild system is based on a custom 24-bit computer, the FST-2. The Tektronix system is based on a DEC PDP11/35 (the OEM version of the PDP/40).

Fairchild sells a $150K system, the Sentinel, and a >$3000K system, the Sentry. The Sentry system is essentially the same as the Sentinel with the following additions: 1) a hard disk instead of floppy disks, 2) much higher timing resolution (156 pscc vs. 1.25 ns), 3) a more general-purpose test head, and 4) a pattern generator for testing memory ICs. Both systems include 8 timing generators (clock phases) and 4K of test-pattern RAM.

All Tektronix systems are >$400K and include hard disks and general-purpose test electronics. The S-3260 is part of the S-3200 family and has 1 ns timing resolution, 7 timing generators (clock phases), 1K of test-pattern RAM, and 1K of test-pattern shift-register memory. Other S-3200 systems are the S-3270 and the S-3275, which include 14 timing generators, 4K test-pattern RAM, 4K of test-pattern shift-register memory, a pattern generator for testing memory ICs, and up to 120 psec timing resolution. The S-3260 can be upgraded to a S-3270 or S-3275 in the future if needed.

The purchase of any of these systems will require us to develop additional software to make the system straight-forward to use and integratable into the fast-turn-around-fabrication system.

On August 11, Jim Leonard of Fairchild submitted a price quotation of $162K for the Sentinel, and on August 20, Terry Walker, Rob Mathews, John Newkirk, and I went to Fairchild to see a demonstration of the Sentinel.

On September 4, Mike Bonham of Tektronix was informed that we were considering buying a Fairchild Sentinel system since our budget maximum was $150K. One week later, Mike Bonham offered us one of their S-3260 systems, a

1-year-old demo system with new system warranties, for the discounted price of $150K (new price >$400K, current value $300K). On September 16, we went to DCA Reliability Labs (a local Tektronix customer) to see a demonstration of a S-3260 system. On September 22, Tektronix formally submitted the quotation, which is valid until October 14 when the machine will be put up for sale at $300K.

That same week, Jim Leonard of Fairchild was notified of the Tektronix offer and of our interest in buying the S-3260 system. On October 1, Jim Leonard and Mike Perugini of Fairchild came to Stanford and made a formal presentation to us on a Sentry VII system. They then delivered a quote of $150K for a reconditioned demo Sentry VII system plus any options that we desire (essenitally a $425K system if new).

By October 1, the Tektronix system appeared to be the better system for our purposes with two possible exceptions:

1) The S-3260 has only 1K of test-pattern RAM (we may need >1K).

2) Fairchild claims that the S-3260 is an unreliable system.

On October 7, in response to our request, Tektronix quoted an additional $11.5K to upgrade the system to a 4K ECl test-pattern RAM. Tektronix also produced a list of 87 S-3200 system customers (over 120 S-3260 systems have been sold since 1972). As of today we have contacted several of these customers regarding their system's reliability. Basically everyone we spoke to is very satisfied with the S-3260 on all counts. There is one exception to this statement. DCA Reliability Labs has a S-3260, the only local S-3200 type system, and they have had considerable maintenance problems with their 6 year old machine. They have only recently gone on a service contract with Tektronix. Tektronix now has the local maintenance support that we need, but this may not have been true earlier. Hughes Aircraft in Southern California says that they

have 95% up-time with their S-3260 and that regular maintenance is very important. Their system, which is used 24-hours-a-day, 5-days-a-week, is never turned off, receives 4 hours per week of routine maintenance, and is calibrated every 6 months. According to several S-3260 owners, the system stays in calibration when recalibrated at the prescribed 6-month intervals.

One of our objections to the Sentry VII system is that it is limited to 60 pins, whereas the S-3260 can test 64 pins. On October 8, Fairchild offered us a Sentry VIII system of the same price of $150K. This is a 120 pin system that they would equip for 64 pins to meet our needs.

After having analyzed each of these systems, we recommend that Stanford purchase the Tektronix S-3260 system with the 1K test-pattern RAM. The use of a 4K RAM would slow testing from the RAM from 18 MHz to 14-15 MHz. Since it is not clear at this time whether we will need more than 1K of RAM, and since the RAMs will not be available for 3-6 months, we feel that the decision to order a 4K RAM should be deferred until we have had more time to analyze our needs. The wafer-prober interface is not included in the $150K price and will cost us about $6K. Since we have not yet made a final decision on which prober to buy, we should also defer the decision of which wafer-prober interface to order for the S-3260. We would like to have a magnetic tape unit on the system. The S-3260 software includes a mag tape interface; however, Tektronix does not sell mag tape units. We recommend the purchase of an 800 BPI mag tape unit from another vendor to connect to the S-3260. The DEC TM-11/TU-10 is a preferred unit if it can be acquired for an acceptable price.

On October 10 Tektronix agreed to pay for shipping for the system to Stanford, and to include all information on disk formats and all system source code with the system. We are still attempting to negotiate a reduced-price

maintenance contract and a guarantee of 95% up-time during the 90-day warranty period. The system will be shipped 6-8 weeks from the date of the purchase order.

The reasons for our choice of the S-3260 are as follows:

1) According to users of these systems, the S-3260 system is better suited to a research and development environment. Hewlett-Packard says the S-3260 is "friendlier" than the Sentry systems and according to Hughes Aircraft, the S-3260 can more easily accomodate unusual testing requirements than the Sentry systems. Both of these companies, plus also the Ford Motor Company, use S-3200 systems in their engineering environments and use Sentry systems in their production environments.
2) The S-3260 is based on the PDP11, which is compatable with our DEC systems. We already have hardware and software that we can use with the S-3260. This is not true for the custom computer of the Sentry.
3) The software on both systems falls considerably short of satisfying our needs; however, since the S-3260 is based on a PDP11, we have the cross-product tools we need to develop additional software. No cross-product tools are available for the Sentry system.
4) The S-3260 has two 1.2 Megabyte, removable cartridge disks, preferable to the single .7 Megabyte, fixed disk on the Sentry system.
5) The S-3260 can make "one-shot" timing measurements, while the Sentry must do a binary search to find the correct time window.
6) Both systems have 2 processors which operate in parallel. The PDP11, in the S-3260 system, and the FST-2, in the Sentry system, control the test configuration and interface with all system

peripherals. These processors initiate the test sequence. Each system also has a microprogrammed processor which is the controller for the test electronics. Programs for these controllers reside in the control store portion of the test-pattern RAM. The S-3260 microprogram word is 32 bits as compared to 16 bits in the Sentry system. Because of this, the S-3260 can perform more parallel functions than the Sentry. Both controllers are pipelined and hence have the common programming problems associated with pipeline processors.

7) The S-3260 (and the S-3270) test controller has only registers for holding subroutine return addresses and loop counters. This is limitation of the S-3260; however, we feel we can live with it. The Sentry test controller has a 16-level-deep stack for the same purpose.

8) The S-3260 has better error handling facilities, e.g., it can record all functional output errors during a test run, while the Sentry can only record which pins had failures on them.

9) The S-3260 test controller has better program branch control, i.e., conditional and indirect branching. The only conditional branch in the Sentry test controller is to the start of a loop.

10) In the Sentry, the functional-test data and the microprogram instructions associated with each line of data are specified in the same program. In the S-3260, the data and the associated instructions are specified in two separate programs. The Sentry approach is preferable in this case and we intend to add additional front-end software to the S-3260 to correct this problem.

11) The S-3260 has a 20 MHz maximum testing data rate, versus 10 MHz for the Sentry.

12) The Sentry has better facilities to redefine the pins of the device-under-test (DUT) on-the-fly. While outputting a test sequence at the full 10 MHz speed, the Sentry can redefine pins from input to output or switch to don't-care status on selected pin outputs. This type of redefinition is needed to test 3-state buses.

The S-3260 can only make these changes while testing at the full 20 MHz if the DUT has less than 64 pins, so that extra pin electronics cards can be used for control information. Also, the DUT interface board would need special wiring for this case. If the DUT has 64 pins and 3-state buses, it can only be tested at a maximum of 5 MHz, since data and control information will be successively sent out the pin electronics cards for the 3-state pins. Additionally, this mode uses 4 times as much test-pattern RAM or shift-register memory.

Also at full speed testing, the Sentry can reconnect any pins to a different timing generator or switch between return-to-zero and non-return-to-zero pulses for selected pins. The S-3260 cannot make either of these reconnections on-the-fly. In each of these cases, we feel the S-3260 will be adequate for our needs. Additionally, if these features become requirements in the future, we could upgrade to the S-3275 test electronics where these features are considerably improved.

13) The S-3260 has faster switching times and smaller pulse abberations. A three-state pad can be switched from input to output only at the beginning of a time cycle on the S-3260 system; this is adequate for our needs. On the Sentry system, this switching can take place at any time other than the start of the cycle, a 10 volt

spike will be sent to the pad. This spike could be reduced to .8v if the CMOS option is purchased. No spikes occur on either system if the switch is made at the beginning of the cycle.

14) One of our requirements is for a tester that can be configured under software control, i.e., where no wiring changes are needed to test circuits with different pin configurations. Both the S-3260 and the Sentry VIII would meet these needs for the most part. A limitation in this regard occurs when > 100 mA (with the Sentry) or > 450 mA (with the S-3260) is needed by the power pins. In that case a specifically wired DUT interface board is needed to connect the power supplies directly to the pins instead of through the pin drivers on the pin electronics cards.

15) The S-3260 wafer-prober interface slows the machine by 30-50%, while the Sentry runs at full speed (it has lower capacitance test heads). However, the S-3260 is still preferred since additional microprobes can be easily connected; it would be more difficult to connect additional probes when using the Sentry.

16) The S3260 provides a +30v to -30v voltage range at the device pins, and all voltages are relative to a common system, chip, and external ground. The Sentry provides a device pin voltage range of +6 to -16v and this is relative to chip ground, which is -11v relative to system and external ground. A Sentry option would give a range to -22v; however, in either case, the Sentry approach is less desirable for our purposes, owing to the problems associated with safely connecting external equipment to the test device.

17) On the S-3260, all pins have independent control of drive and sense voltages, which permits easier testing of hybrid technology parts. The Sentry has only 4 drive voltage pairs and 1 sense voltage pair.

18) The Sentry has more timing phases and any timing generator can be connected to any pin. Of the 7 timing generators on the S-3260, each pin can only select between two. However, the S-3260 is adequate for our needs and 7 more timing generators can be added to the system.

19) The 50-ohm external-access matrix of the S-3260 is expected to be important to future testing demands. Such a matrix is not available on the Sentry.

20) Both the S-3260 and the Sentry have a foreground and a background mode of operation. With this feature these systems can be simultaneously used to develop new test programs while running a device test; a useful capability for us. According to Ford Motor Company and Hewlett-Packard, this feature is "very powerful" on the S-3260 and is not satisfactory on the Sentry.

See Appendix 4 for a chart that compares the Sentry and the S-3260 systems.

APPENDIX 1

IC TESTER SPECIFICATIONS

1. Interactive functional testing of packaged chips and wafers
2. Performance (timing) measurements
3. Testing of dynamic designes - requires 2 MHz minimum data rate 10-20 MHz preferred
4. Testing of NMOS, CMOS, and TTL circuits - digital and linear
5. 64 pin capability
6. Configuration process under software control
7. Integratable into fast-turn-around-fabrication system:
   - A. Same test vectors for simulator and tester
   - B. Can be controlled by remote computer
8. Straight-forward to use, easy to program, high-level language
9. Reliable and easy to maintain
10. Able to synchronize testing to internal chip clock - Able to bring outside signals to chip under test
11. Maximum cost - $150K

APPENDIX 2

MACHINE TYPES

MEMORY TESTERS ONLY:

ACCUTEST
MACRODATA TEST SYSTEMS

PCB TESTERS ONLY:

JOHN FLUKE MANUFACTURING CO.
PLANTRONICS/ZEHNTEL

FILM THICKNESS TESTER ONLY:

PROCESS CONTROL CORP.

DC PARAMETRIC TESTERS ONLY:

LOMAC CORP.
LORIN
AUTOMATED TECHNOLOGY
HHH

GENERAL PURPOSE MEASUREMENTS SYSTEM ONLY:

HEWLETT-PACKARD

TEST HEADS AND OTHER COMPONENTS ONLY:

AUTEK

GENERAL PURPOSE FUNCTIONAL TEST AND MEASUREMENT SYSTEMS:

TEKTRONIX
FAIRCHILD
TERADYNE
MEGATEST
GENRAD
SIEMENS
MICROCOMPONENT TECHNOLOGY
BEC, INC.

APPENDIX 3

GENERAL PURPOSE FUNCTIONAL TEST AND MEASUREMENT SYSTEMS

MSI Testers

BEC, Inc. - $3.2K, 16 pin only
Siemens - $38K, 24 pins, 1 MHz

LSI - Bench-Top Testers (Production Oriented)

GenRad - $30K, 48 pins, 2 MHz
Microcomponent Technology - $?, 48 pins

LSI Testing Systems

Megatest - $125K, 40 pins, 10 MHz
Needs wiring setup for each chip type, production oriented

Teradyne - $250K, 84 pins, 6 MHz
Mostly analog tester, hard to generate digital test vectors

Fairchild - $150K & $300K, 60 pins, 10 MHz
Meets many of our needs

Tektronix - $400K (to us $150K), 64 pins, 20 MHz
Meets most of our needs

APPENDIX 4

PARAMETER	TEKTRONIX	FAIRCHILD
Pin Electronics Range Drive and Sense	V_H: +30 to -10 V_L: +10 to -30 $V_H - V_L \leq 30$ V	+6 to -16; relative to TCOM at -11 V
Drive — Resolution	10 mV	10 mV
Drive — Accuracy	20 mV ± .25%	15 mV ±.1%
Switching Mode Current	±100 mA	±100 mA
Supply Mode Current	±450 mA	±100 mA
Drive Speed t_r 10 pF load	13 ns (Δ= 30 V)	40 ns (Δ= 30 V)
t_{inh}	9 ns	50 ns
Inhibit Aberration	200 mV	10 V
Sense — Range	±5, ±30V	+6 to -10, +6 to -16V
Sense — Resolution	1.67, 10 mV	10 mV 40 mV
Sense — Accuracy	±.17% + 1% of range	.08% ± 10 mV
Sense — Z in	2 MΩ/12 MΩ	Ib < 100 nA
Sense — C in	25 pF / 14 pF	25 pF
Drive C out	60 pF	40 pF
Drive Voltages	All pins independent	4 pairs
Sense Voltages	All pins independent	1 pair
Drive Phases	5 total; 2 per pin (ϕD to all + quadrants)	6 total; to all pins
Sense Phases	2 total; to all pins	2 total; to all pins
Pin Pattern Memory	1K Shift Register 1K/4K PRAM	4K PRAM
Timing Generator Period Range Period Resolution Pulse Resolution	48 ns - 16 µs; 2 µs - 1 ms 8 ns ; .5 µs 1 ns ; .5 µs	100 ns - 41 µs; 41 ms 10 ns ; 10 µs 156 ps ; 10 µs
Timing Skew at pins	±1 ns	±1 ns

APPENDIX 4 cont'd

PARAMETER	TEKTRONIX	FAIRCHILD
External Access	4 ea. 50 Ω lines through matrix to pins. Direct or buffered.	None. Tester Common TCOM at -11 V
DUT Time Measurement	One Shot	Binary Search
Prober Interface	18" cable	Mounts on top or use cable
DUT Power Supplies	up to 8 (4 minimum)	3
CPU	PDP 11/35	24 bit custom
DISK	2each 1.2 M byte cartridge	.7 M byte fixed
Maximum Functional test rate	20 MHz	10MHz
CPU access to DUT for universal programming of signals and power	64 pins	60 pins (>60 pins requires Sentry VIII)

VLSI DEVICE RESEARCH

7/1/80 to 12/31/80

MODELING OF DEPLETED BASE BIPOLAR STRUCTURES

J. M. C. Stork

One of the operational limits encountered in scaling the vertical dimensions of bipolar transistors is punchthrough of the base. In this case, a neutral base region does not exist anymore, and the collector current becomes a strong function of collector voltage, thereby reducing the maximum available gain.

Recently [1], Japanese researchers introduced the bipolar mode SIT: a normally-off, short channel, vertical JFET (see Fig. 1), that, when operated with a forward biased gate (base), shows DC characteristics similar to a high output conductance bipolar transistor. No neutral channel is present; instead a potential barrier arises, which can be modulated by either the gate or the drain potential, both resulting in an exponential dependence of current on applied voltage.

This general type of behavior is observed in all device structures, whether of the MOS, JFET or Bipolar configuration, as they are scaled to very small physical dimensions. A typical energy band diagram, as shown in Fig. 2, indicates the presence of a saddle point in the potential. Identifying this region of vanishing electric field as the "control" region, a generally applicable model for the transport current at low current levels is developed, giving the following current expression (neglecting recombination):

$$I_{DS} = qD_n N_s Z \cdot \frac{W_{eff}}{L_{eff}} \exp\ (-q\psi_B / kT)$$

with

$$W_{eff} = \int_{-w/2}^{w/2} \exp\Big(- q \left(\psi^* - \psi\ (x,y^*)\right) / kT \Big) dx$$

$$\text{and} \qquad L_{eff} = \int_{0}^{\ell} \exp\left(-q\left(\psi(y,o) - \psi^* \right) / kT \right) dy$$

It is the saddle point potential (ψ^*) that controls the current flow and leads to an exponential dependence of current on applied voltage. In a conventional bipolar transistor, the potential barrier (ψ_B) consists of the built-in potential of the emitter-base junction and is directly accessible at the base contact. Hence maximum efficiency in modulating the barrier by the base terminal is achieved: $n \equiv \frac{-\Delta\psi_B}{\Delta Vbe} = 1$. In the MOS and SIT transistors the saddle potential is not directly accessible. The surface potential in MOS transistors is reduced from the gate voltage by the presence of the oxide; in a SIT the saddle potential in the channel takes values between 0.3 and 1.1 eV. The resulting non-ideal exponential characteristics have a lower efficiency of the gate ie. $n > 1$, and are strongly influenced by device geometry and doping profiles.

The present work has concentrated on how to optimize the efficiency of the above mentioned devices for VLSI applications. Specifically, the sensitivity of the current in the structure of Fig. 1 to variations in processing variables has been investigated through 2D computer simulations and experiment. A measurement technique has been developed to extract the value of the potential barrier when no direct electrical connection is possible.

Accurate calculation of the parameters ψ_B, W_{eff}, L_{eff} is possible only through 2D numerical simulation [2]. When current flow is small, the potential will not be affected by the charge and only Poisson's equation needs to be solved. To enable comparison with analytical solutions [3], initial calculations were done using the "ideal" device structure shown in Fig. 3.

From this work it was concluded that the presence of mobile carriers (especially holes) at the control region is particularly important in determining the device characteristics. The efficiency of modulating the potential barrier by the gate (base) voltage (1/n) will only be larger than 0.5 if the barrier height (ψ_B) exceeds 0.5 eV. This implies that the hole concentration must exceed the electron density at the saddle point. Or, in other words: a sufficiently steep exponential characteristic ($1/n > 0.5$) requires the presence of a p-type control region: an "induced" base. This condition can be reached, however, just by the presence of two closely spaced external base regions due to the "spill over" of holes into the lightly doped channels as shown in Fig. 3. Thus the position of the electrical junciton (ie. where n = p) rather than the metallurgical junction position is essential in determining the low current slope.

Subsequent simulations of realistic device structures showed similar results. Specifically it was found that the potential barrier height is very sensitive to the lateral spacing between the gates, implying that tight control of photolithography may be necessary to obtain reproducible device characteristics. Most importantly, it has been found that the efficiency factor (determining transconductance and output conductance) is uniquely specified once the potential barrier is known, independent of the specific choice of N_{epi}, X_j and W. Different geometries and doping levels which lead to the same potential barrier height, also lead to substantially the same electrical device characteristics (Fig. 4).

Since no direct electrical connection to the saddle potential is possible, its value must be extracted by other means. Because the barrier acts like an activation energy however, its height can be extracted from the slope of the extrapolated transport saturation current versus the inverse of absolute temperature [4].

DC characteristics (including temperature as a parameter) were measured on SIT structures (see Fig. 1), fabricated in the following technology: 4 μm thick n-type epitaxial layers of different resistivities (1-10-20-30 Ω cm) were grown on heavily doped, (100) oriented, n-type substrates. The channel opening was defined by the resist masking the boron implantation for the extrinsic base regions. Subsequent local oxidation of the base provided self-alignment of the emitter region. The linewidths of the nitride were varied from 2.5 to 3.75 μm with 0.25 μm increments. The lithography was done with a CANON FPA-141 4:1 projection aligner. The base-collector junction depth was chosen such as to obtain pure bipolar transistors for the smallest geometry due to lateral overlap of the base diffusion, whereas the largest spacing would result in JFET behavior, as shown in Fig. 5. For the intermediate values, so called "SIT" behavior is observed.

The experiments confirm the theoretical predictions described above. Especially for the lower epilayer resistivities, the transfer characteristics are extremely sensitive to variations in emitter width; the low current slope decreases from the ideal bipolar transistor case, corresponding with a reduction in barrier height and the efficiency factor is indeed found to be uniquely specified by the potential barrier height.

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H. Stork, J. D. Plummer, C. Ho, Laboratory Report EE 412, 1979, Stanford University.

[4] D. Takacs, ea, IEDM Tech. Digest, 1980, p. 569.

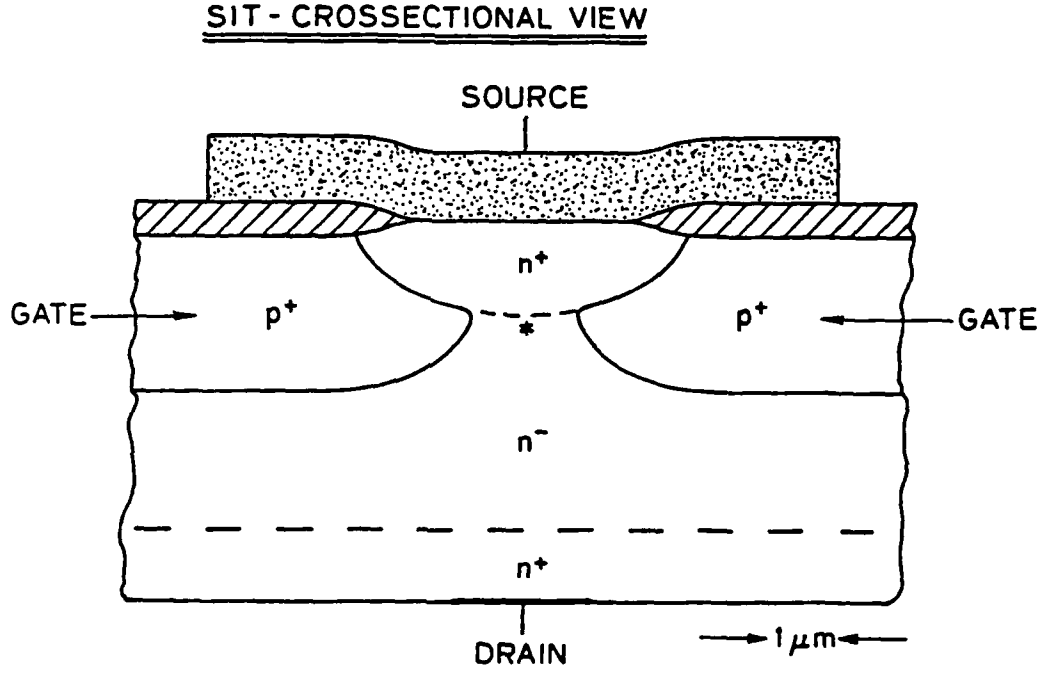
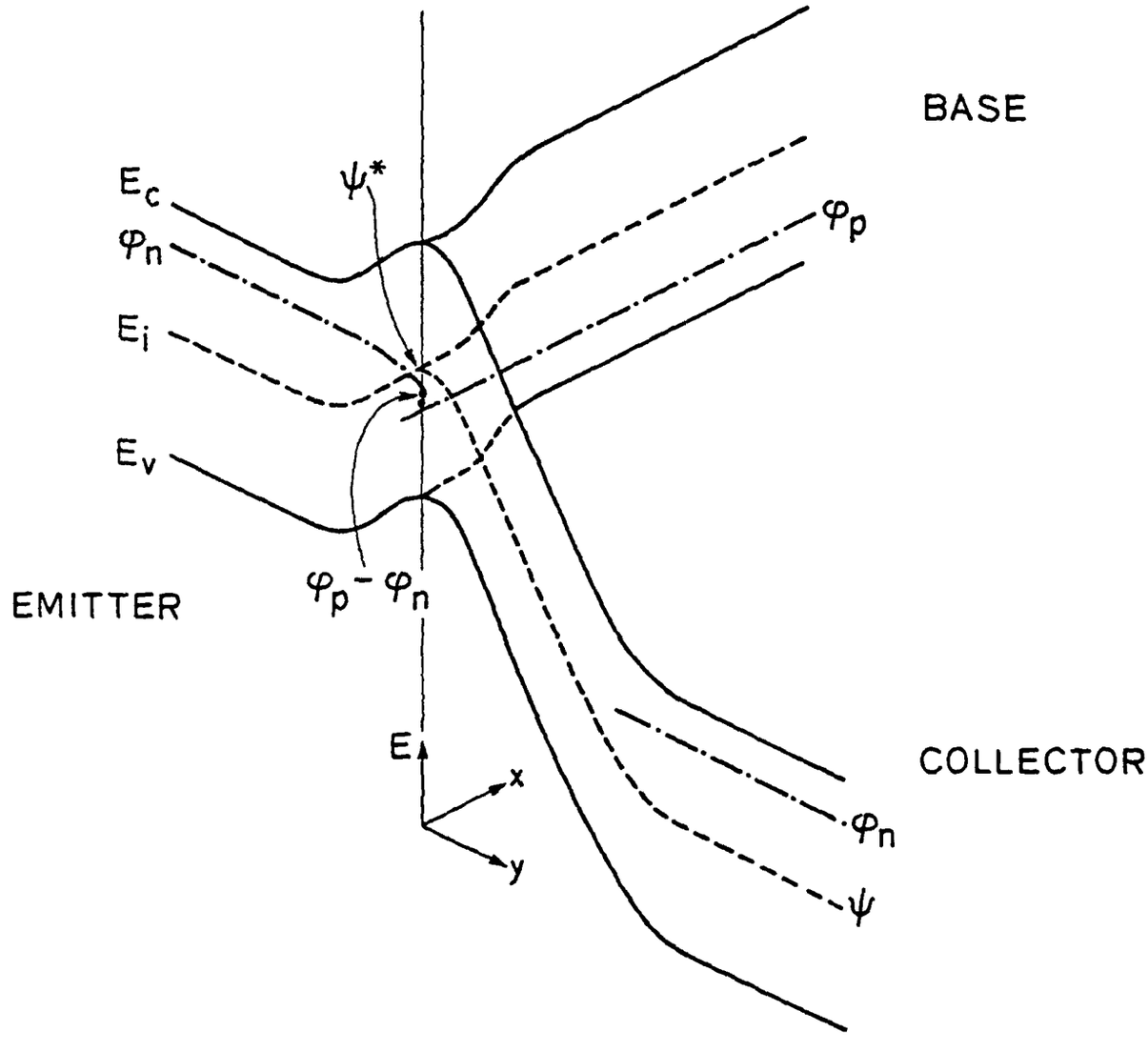


Fig. 1 Cross-section of a SIT transistor. The source is self-aligned through the use of composite masking and local oxidation. The extent of lateral diffusion from the gate determines the saddle potential in the channel (*).

★ ENERGY BAND DIAGRAM ★



$$I_c = qD_n N_s \cdot Z \cdot \frac{W_{eff}}{L_{eff}} \cdot e^{-q\psi^*/kT} (1 - e^{-qV_{ce}/kT})$$

W_{eff}, L_{eff} ⟷ CURVATURE IN POTENTIAL SADDLE POINT

Fig. 2. Typical energy band diagram.

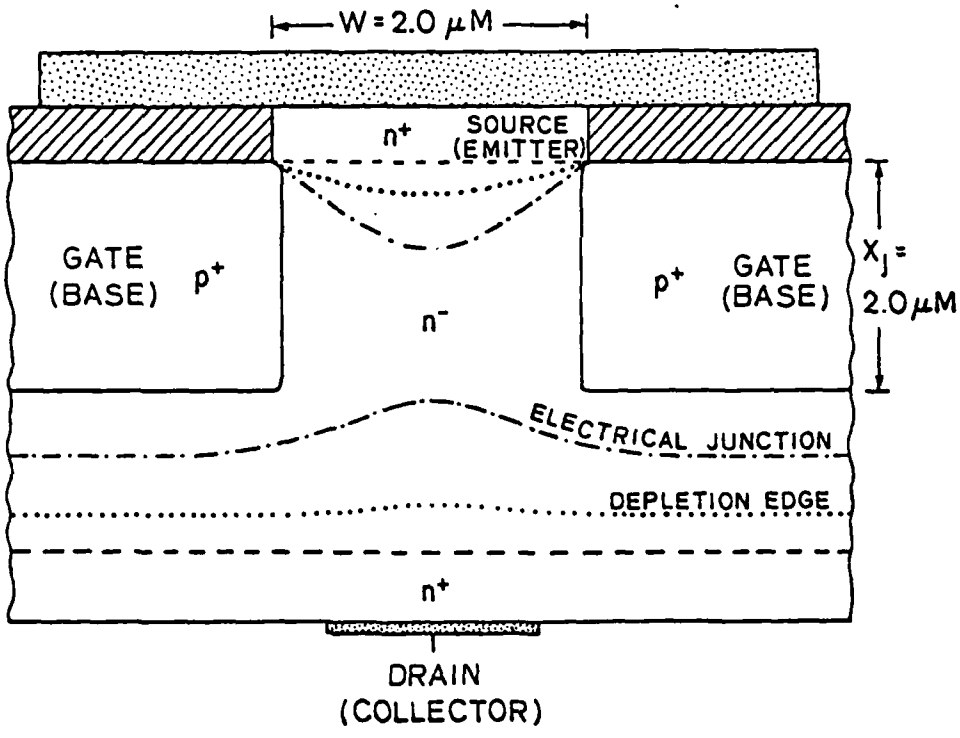


Fig. 3. "Ideal" device structure: uniformly doped profiled and abrupt junction. The channel is depleted form electrons and totally p-type (ie. p > n).

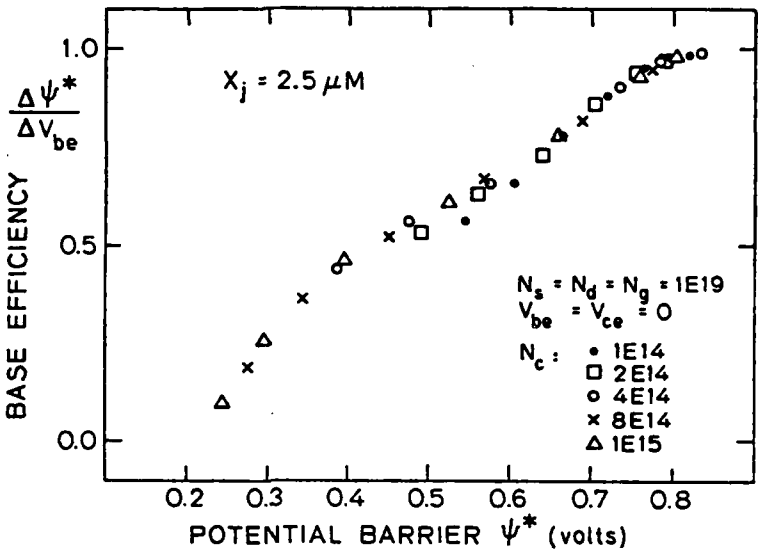


Fig. 4a. Base efficiency versus potential barrier height with epi layer doping level as the parameter, determined from 2D computer simulations.

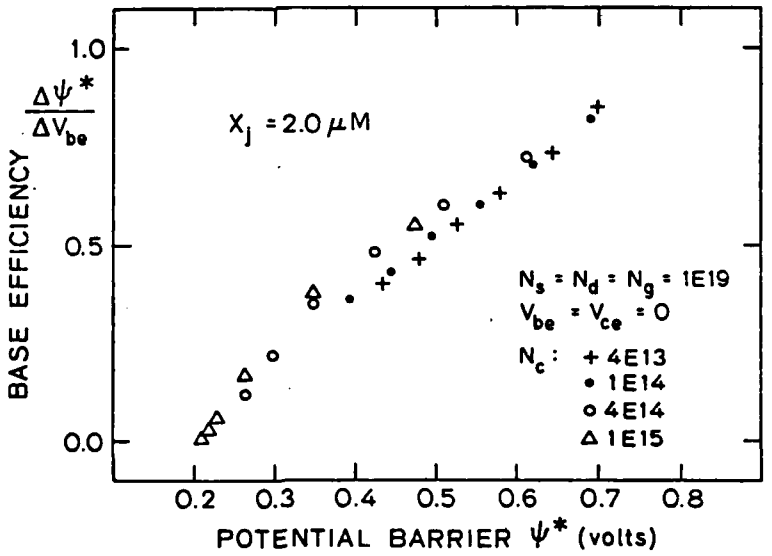


Fig. 4b. The same figure as Fig. 4a, but now for a junction depth of 2.0 μm.

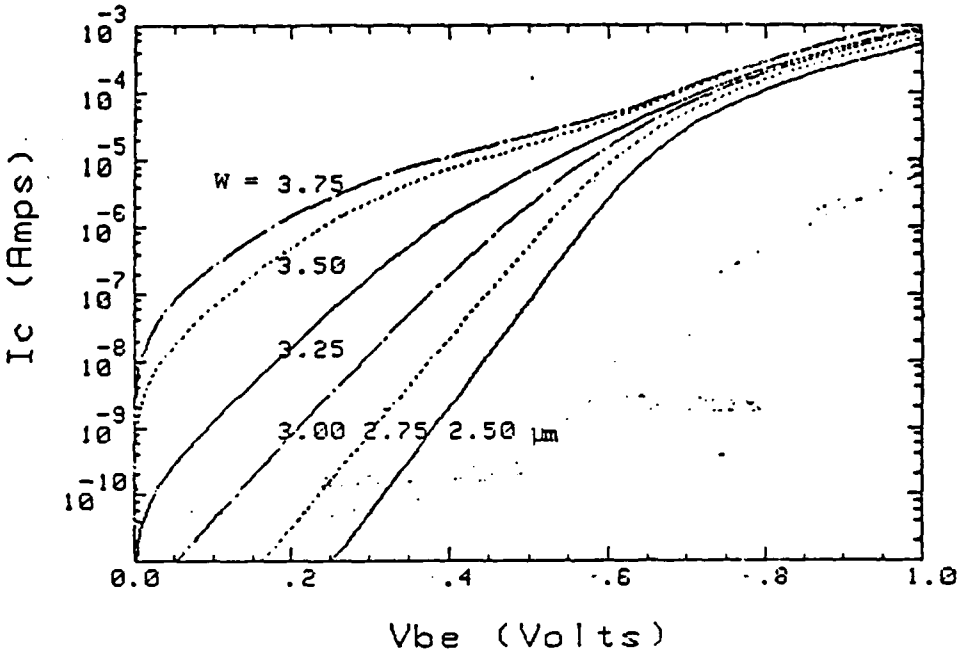


Fig. 5a Collector current as a function of base-emitter voltage for neighboring devices with different emitter widths. The transition from pure bipolar operation (W=2.5 µm) to JFET behavior (W > 3.5 µm) is clearly shown. The intermediate region shows SIT (depleted base) operation.

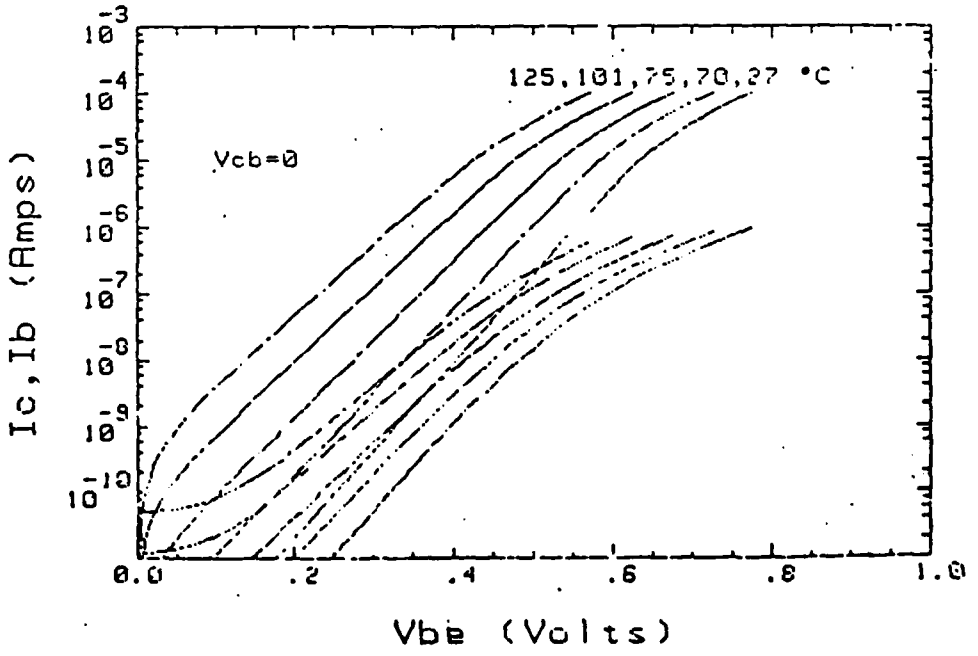


Fig. 5b Collector and base currents for one particular device with temperature as the parameter. Plotting the collector current versus inverse temperature enables extraction of the barrier height corresponding to a certain emitter width. A unique relation is found between the ideality factor n and the potential barrier height, independent of the choice of N_{epi}, X_j and W.

THE EFFECT OF METALIC PRECIPITATES ON THE I-V CHARACTERISTICS OF BIPOLAR TRANSISTORS AND DIODES[1]

R. B. Lefferts, R. M. Swanson, and J. D. Meindl

The recombination current due to metalic precipitates in the space-charge region of silicon diodes has been calculated for both forward and reverse bias conditions. Excellent agreement between calculations and experimental data has been obtained in modeling both the space-charge recombination component of forward base current and the base emitter reverse characteristic on an NPN transistor in the current range 10^{-14} to 10^{-4} Amps.

Metal precipitates have been found to cause excess reverse currents in silicon diodes at voltages significantly below avalanche.[2] Previous modeling of this leakage component has been based on a Fowler-Nordhiem field emission mechanism.[3] Unfortunately, the particle potential due to charge accumulation was not considered in this analysis and a balance between electron and hole emission currents, as is necessary in steady state, was not established. Although metalic precipitates have been used to model the reverse I-V characteristic, no calculation has been presented concerning the role of precipitates on the forward characteristics of diodes and transistors.

In this work, the influence of spherical metal precipitates on the I-V characteristics of devices has been analyzed and compared to experiments. The exact potential distribution around a metal particle, including the image potential near a floating metal sphere, is used in the model to calculate the capture and emission of carriers. Energy dependent tunneling is included in the analysis using the WKB approximation so that thermionic emission, thermionic field emission, and Fowler-Nordhiem emission are simultaneously incorporated. The potential of the precipitate is calculated by establishing a balance between electron and hole currents. The model, when applied to an abrupt PN junction under forward bias, predicts recombination currents which fit the experimentally observed relation $I \sim e^{qV/mkT}$. The m factor is found to depend mainly on precipitate radius, going from 1.6 at 10 Å to 1.1 at 150 Å. Under reverse bias, the model agrees with observed leakage currents $I \sim V^n$ where $n \sim 1$ at low voltage and reaches ~7 near avalanche.

This model has been applied at room temperature to NPN transistors fabricated using a linear compatible I^2L process. Good agreement between theory and experiment for both forward and reverse bias is obtained for precipitates with radii between 25 and 50 Å and densities on the order of $10^{10}/cm^3$.

This new model for PN junctions under low forward bias and reverse bias provides a new physical interpretation of the space-charge recombination current in transistors and diodes. Metalic precipitate recombination plays a major role in devices operating at low currents.

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[1]This work was supported under DARPA Contract No. MDA903-80-C-0432.

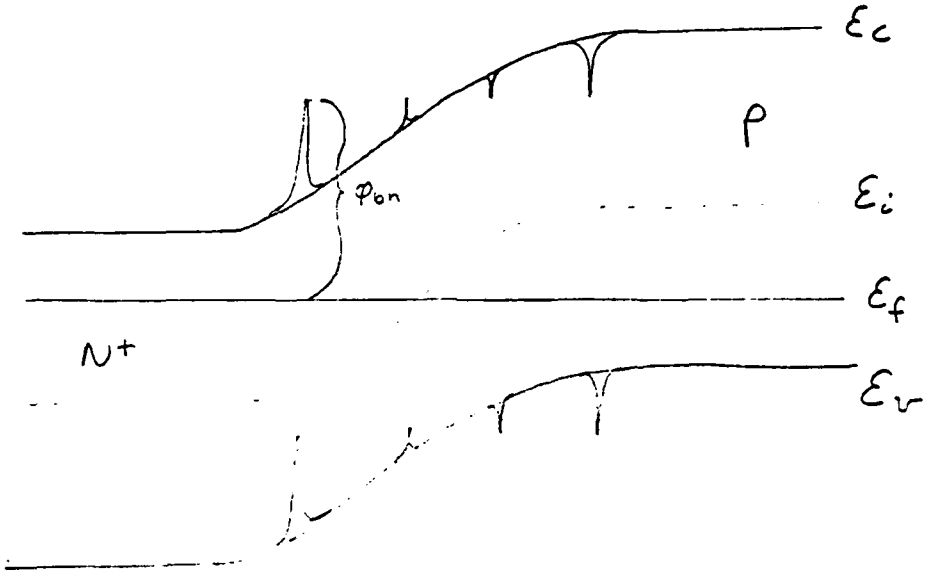
[2]A. Goetzberger and W. Shockley, J. Appl. Phys., Vol. 31, No. 10, p. 1821, 1960.

[3]H. H. Busta and H. A. Waggener, J. Electrochem. Soc., Vol. 124, No. 9, p. 1424, 1977.

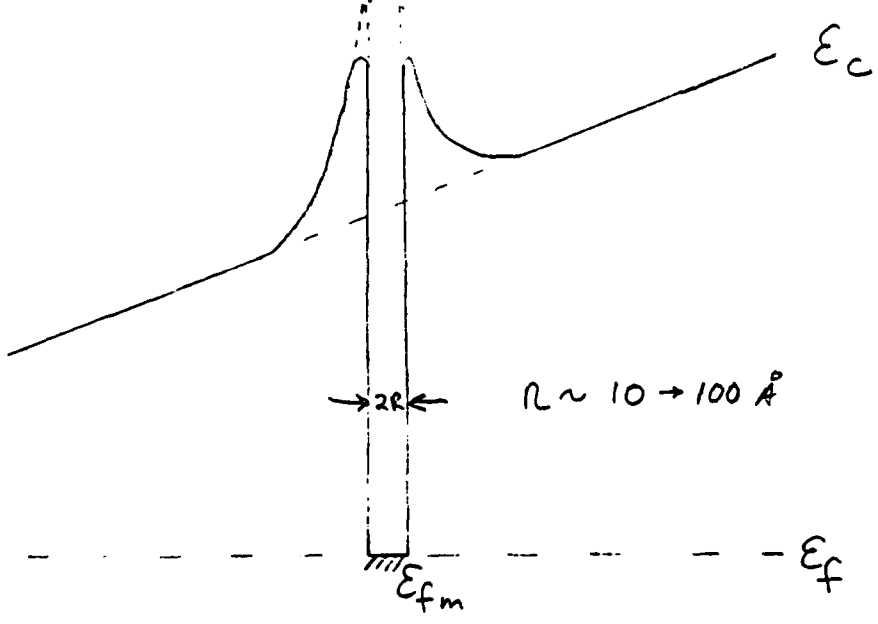
Supplementary Material

Equilibrium Band Diagram

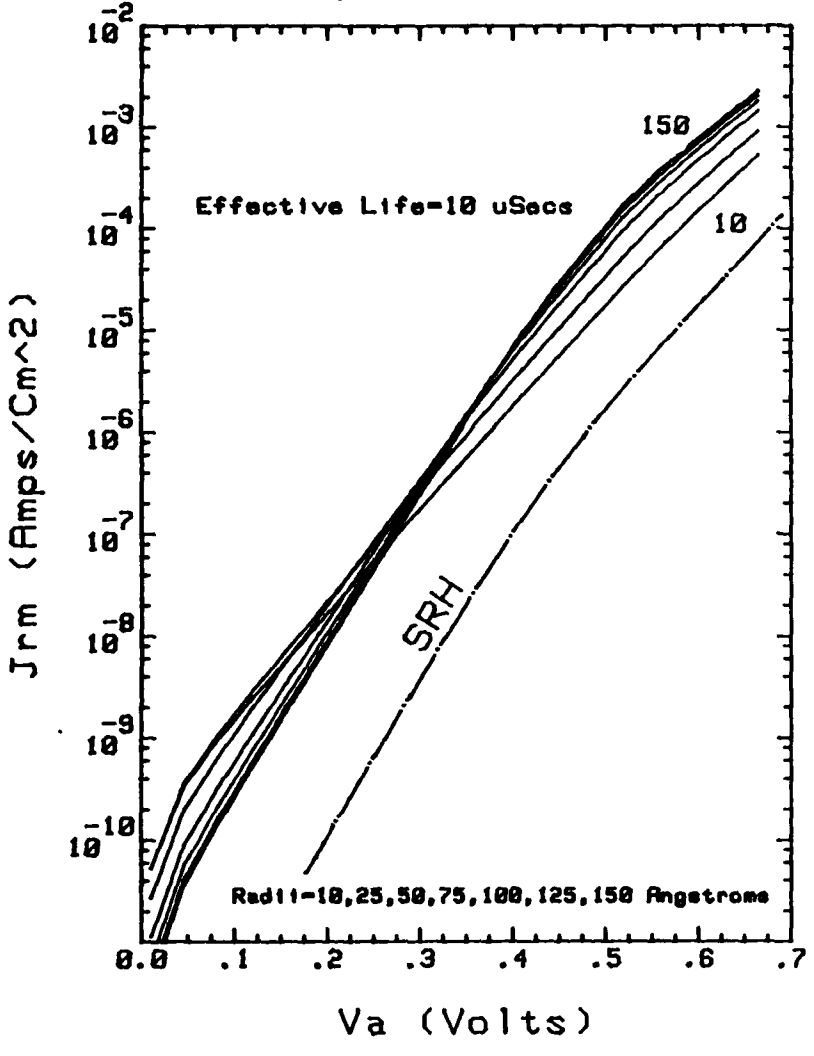
(Precipitates in Depletion Region)



Potential Near Precipitate



Forward IV Characteristic (Calculated)
Metalic Precipitate Recombination Model



m Factor Extracted from Calculated IV
Metalic Precipitate Recombination Model